Claims

1. A structure comprising:

a first substrate and a second substrate; and

first solder bumps and second solder bumps therebetween, wherein said second solder bumps have at least a portion that melts at a substantially lower temperature than said first solder bumps.

2. A structure as recited in claim 1, wherein said second solder bumps are larger than said first solder bumps.

3. A structure as recited in claim 1, wherein said second solder bumps comprise a portion having a higher concentration of tin than does said first solder bumps.

4. A structure as recited in claim 3, wherein said portion comprises an eutectic concentration of tin.

5. A structure as recited in claim 3, wherein said portion is adjacent to said second substrate.

6. A structure as recited in claim 3, wherein said portion is centrally located within said second solder bump.

7. A structure as recited in claim 3, wherein said portion is said entire second solder bumps.

8. A structure as recited in claim 1, wherein said second solder bumps are for aligning said first substrate and said second substrate before melting said first solder bumps.

9. A structure as recited in claim 8, wherein said second solder bumps are larger than said first solder bumps.

10. A structure as recited in claim 1, wherein said second solder bumps melt at a temperature at least 25C less than said first solder bumps.

11. A structure as recited in claim 1, wherein said first substrate comprises a first semiconductor chip.

12. A structure as recited in claim 11, wherein said second substrate comprises a second semiconductor chip.

13. A structure as recited in claim 12, wherein said second chip is larger than said first chip.

14. A structure as recited in claim 12, wherein said second chip further comprises wire bond pads for bonding to a printed circuit board.

15. A method of joining, comprising:

(a) providing a first substrate and a second substrate; and

(b) providing first solder bumps and second solder bumps connecting said first substrate and said second substrate, wherein said second solder bumps have at least a portion that melts at a substantially lower temperature than said first solder bumps.

16. A method as recited in claim 15, wherein said providing (b) comprises providing said second solder bumps larger than said first solder bumps.

17. A method as recited in claim 15, wherein said providing (b) comprises providing said second solder bumps with a portion having a higher concentration of tin than said first solder bumps.

18. A method as recited in claim 17, wherein said portion comprises a eutectic concentration of tin.

19. A method as recited in claim 17, wherein said providing (a) comprises providing said first substrate with identical solder bumps at all positions and providing said second substrate with solder bumps comprising a higher concentration of tin at locations of said second solder bumps than at locations of said first solder bumps.

20. A method as recited in claim 20, wherein said providing (a) comprises providing said second substrate with solder bumps consisting exclusively of tin exclusively at locations of said second solder bumps.

21. A method as recited in claim 15, wherein said first and said second solder bumps provide mechanical connection between said first substrate and said second substrate.

22. A method as recited in claim 20, wherein said first solder bumps provide electrical connection between said first substrate and said second substrate.

23. A method as recited in claim 15, wherein said providing (b) comprises:

(b1) mounting said first substrate on said second substrate;

(b2) heating to melt at least a portion of said second solder bumps without melting said first solder bumps wherein after said melting said first substrate aligns with said second substrate;

(b3) heating to melt at least a portion of said first solder bumps to form said joining, wherein said first solder bumps wet contact on wet contact and wherein said second solder bumps align said first substrate and said second substrate before melting of said first solder bumps.

24. A method as recited in claim 15, wherein said second solder bumps are larger than said first solder bumps.

25. A method as recited in claim 15, wherein said second solder bumps melt at a temperature at least 25C less than said first solder bumps.

26. A method as recited in claim 15, wherein said first substrate comprises a first semiconductor chip.

27. A method as recited in claim 26, wherein said second substrate comprises a second semiconductor chip.

28. A method as recited in claim 27, wherein said second chip is larger than said first chip.

29. A method as recited in claim 28, wherein said second chip further comprises wire bond pads for bonding to a printed circuit board.

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